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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,561	07/26/2002	Kent Kuohua Chang	9167-US-PA	1295

31561 7590 08/06/2003

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
LINDSAY JR, WALTER LEE

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Appli ant(s)	
	10/064,561	CHANG, KENT KUOHUA	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-30* is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-12 and 14-17* is/are rejected.

7)☒ Claim(s) *4,9,13 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

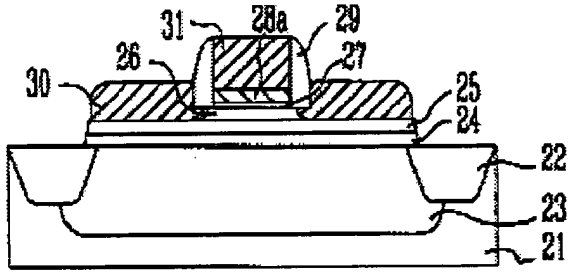
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5-7, 10 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee U.S. Patent No. 6,406,973.

Lee discloses the use of a SiGe elevated source/drain.

FIG. 2D



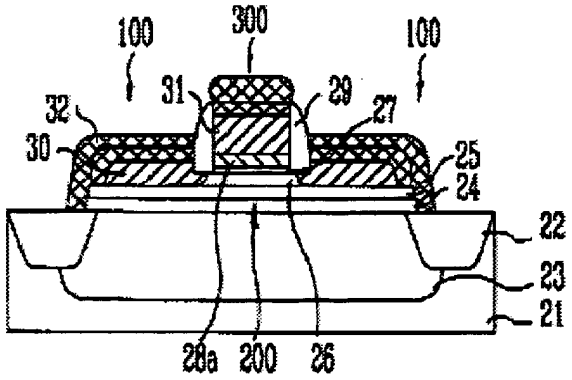
Referring now to FIG. 2D, the native oxide film is removed by the second cleaning process. Then, an **epi-SiGe layer 30 and a poly-SiGe layer 31** are simultaneously formed on the exposed portions of **the SiGe layer 25 and the remaining gate polysilicon layer pattern 28a, respectively, by selective SiGe growth process**.

In the above, the second cleaning process includes an ex-situ cleaning process, and an in-situ cleaning process performed in the epitaxial silicon equipment. The ex-

situ cleaning process is performed by RCA cleaning process or a combination of ozone cleaning process and HF dipping process. The in-situ cleaning process includes performing a hydrogen bake of 800 through 900° C. for 1 through 5 minutes before the epi-SiGe layer 30 and the poly-SiGe layer 31 are formed, thus preventing generation of any oxide films.

In case of a low-pressure chemical vapor deposition (LPCVD) method, the selective SiGe growth process includes the following deposition conditions: the deposition gases use DCS and HCl, upon deposition, DCS is 30 through 300 sccm and HCl is 30 through 200 sccm wherein **GeH_4** of 30 through 300 sccm is introduced together for Ge doping. Also, the deposition pressure is about 10 through 50 Torr and the deposition temperature is 750 through 950° C. In case of an ultra high vacuum chemical vapor deposition (UHVCVD) method, the selective SiGe growth process includes the following deposition conditions: the deposition gases use **SiH_4 or Si_2H_6 wherein GeH_4** of 30 through 300 sccm is introduced together for Ge doping. Also, the deposition pressure is less than 1 Torr and the deposition temperature is 600 through 750°C. **The thickness of the epi-SiGe layer 30 and the poly-SiGe layer 31 formed under these conditions is about 500 through 1000 Angstrom**.

FIG. 2E



Referring now to FIG. 2E, an ion implantation process for source/drain formation and gate doping is performed. Then, a Ti layer is deposited on the entire structure and is then experienced by first annealing process, thus forming a **$TiSi_2$ layer** 32 at the exposed portions of the epi-SiGe layer 30 and the poly-SiGe layer 31. Then, some of the Ti layer that was not reacted is removed by first annealing process, thus completing a $TiSi_2$ layer 32 by second annealing process. Thus, a buried/elevated junction 100, in which the first Si layer 24, the SiGe layer 25, the epi-SiGe layer 30 and the $TiSi_2$ layer 32 are sequentially stacked, is formed. Also, an elevated channel 200, in which the first Si layer 24, the SiGe layer 25 and the second Si layer 26 are sequentially stacked, is defined. Further, a gate electrode 300, in which the remaining gate poly-silicon layer pattern 28a, the poly-SiGe layer 31 and the $TiSi_2$ layer 32 are sequentially stacked, is formed,

In the above, the ion implantation process for source/drain formation and **gate doping injects BF_2 ions of dose of 1E15 through 1E16 ions/cm^2 at the energy of 10 through 40 KeV**. The $TiSi_2$ layer 32 is formed by depositing the Ti layer in thickness of 100 through 300 Angstrom, firstly performing a rapid thermal annealing

(RTA) at the temperature of 500 through 700°C., using wet etching solution such as SC-1 etc. to remove any of the Ti layer that was not reacted and then secondly performing a rapid thermal annealing process at the temperature of 750 through 850° C (col. 4 lines 15-col. 5 lines 8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,406,973) in view of Chu et al. U.S. Patent No. 6,426,265.

Lee is applied earlier in this writing but likes the anticipation of forming the SiGe layer formed of RTCVD.

Chu discloses the use of RTCVD process to form a SiGe layer and is shown to show that this method is acceptable in the growth of SiGe layers.

In accordance with the present invention, the SiGe base layer may be formed by utilizing UHVCVD, MBE, **RTCVD,** PECVD or another like deposition process which is capable of **epitaxially forming such a SiGe layer**... (col. 4 lines 51-56).

In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the **RTCVD** method of Chu in the

primary reference of Lee in order to improve the electric characteristics of the transistor in order to form an elevated source/drain.

5. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,406,973) in view of Yeo et al. U.S. Patent No. 6,492,216.

Lee is applied earlier in this writing, but lacks the anticipation of forming a metal silicide of cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

Yeo discloses a metal silicide made of cobalt or nickel in order to show that cobalt silicide or nickel is a legitimate form of silicide.

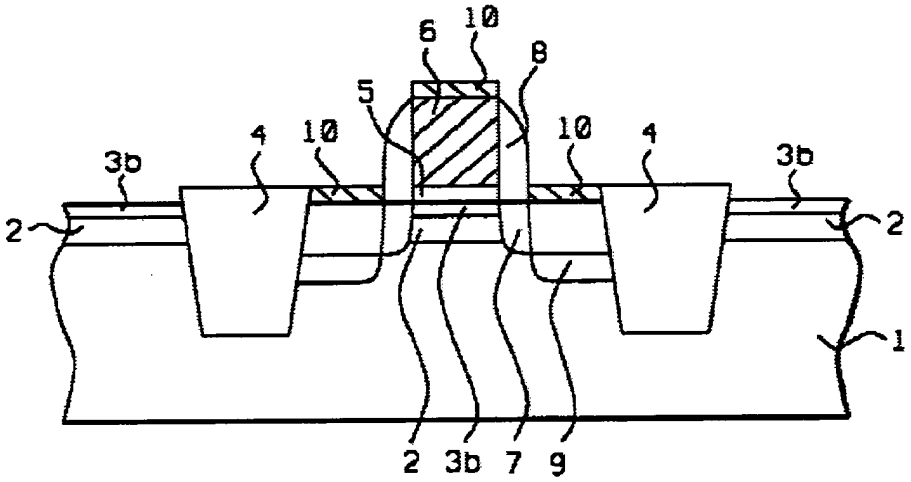


FIG. 6

Metal silicide regions 10, shown schematically in FIG. 6, are next selectively formed on exposed portions of polysilicon and silicon. A metal layer such as titanium, tantalum, tungsten, nickel, or cobalt, is first deposited via plasma vapor deposition (PVD) procedures, at a thickness between about 20 to 200 Angstroms. RTA procedures are next employed at a temperature between about 400 to 700° C., for a

time between about 5 to 60 sec, to form metal silicide regions 10, on polysilicon gate structure 6, and on heavily doped source/drain region 9. Portions of unreacted metal, located on insulator spacers 8, and on STI regions 4, are selectively removed via wet etch procedures, using a solution comprised of $H_2 O_2$ --HCl--NH_4 OH--$H_2 SO_4$. Metal silicide regions 10, comprised of either titanium silicide, tantalum silicide, tungsten silicide, **nickel silicide**, or **cobalt silicide**, are formed on the portions of heavily doped source/drain region 9, located in silicon capping layer 3b, and in silicon-germanium-carbon layer 3 (col. 5 lines 26-43).

In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicide formed of cobalt or nickel in the primary reference of Lee in order to form a channel region for a MOSFET device, via use of a semiconductor alloy mainly because the primary reference also uses a silicide layer.

Allowable Subject Matter

6. Claims 21-30 are allowed.

7. Claims 4, 9, 13 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming a gate structure on a substrate, the gate structure having a capping layer thereon;

forming a source/drain with a shallow-junction in the substrate beside the gate structure;

forming a spacer on sidewalls of the gate structure;

forming an elevated SiGe source/drain layer on the source/drain with a shallow junction;

removing the capping layer; and

forming a metal silicide layer on the gate structure and the elevated SiGe source/drain layer, as required by claim 21.

The prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the RTCVD is conducted under 1~20 Torr and 500°C as required by claims 4 and 13 as they depend from claims 2 and 11 respectively.

The prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein an implanting energy for forming the source/drain with a shallow junction is 2~3KeV, as required by claim 9 and 18 as they depend from claims 1 and 10 respectively.

Lastly the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the capping layer and the spacer comprise the same material, as required by claim 19 as it depends from claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (703) 306-5727. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-3325.

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

July 24, 2003